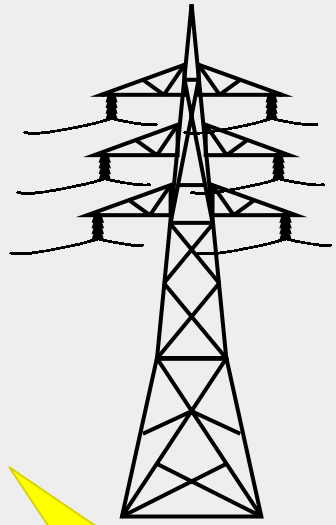
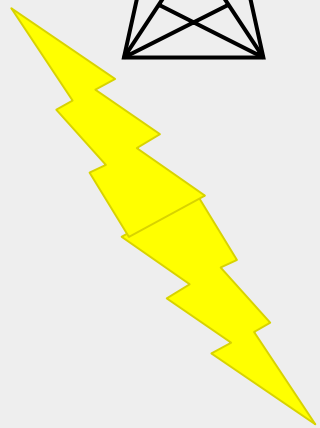
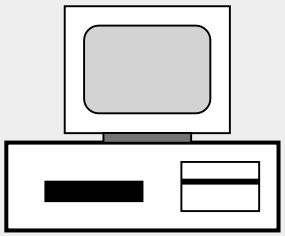
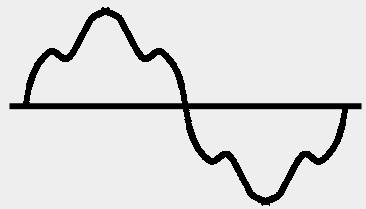
TAS Power-Tech.

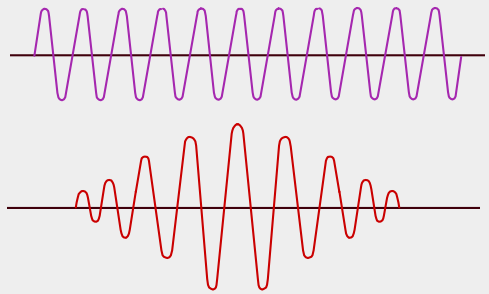








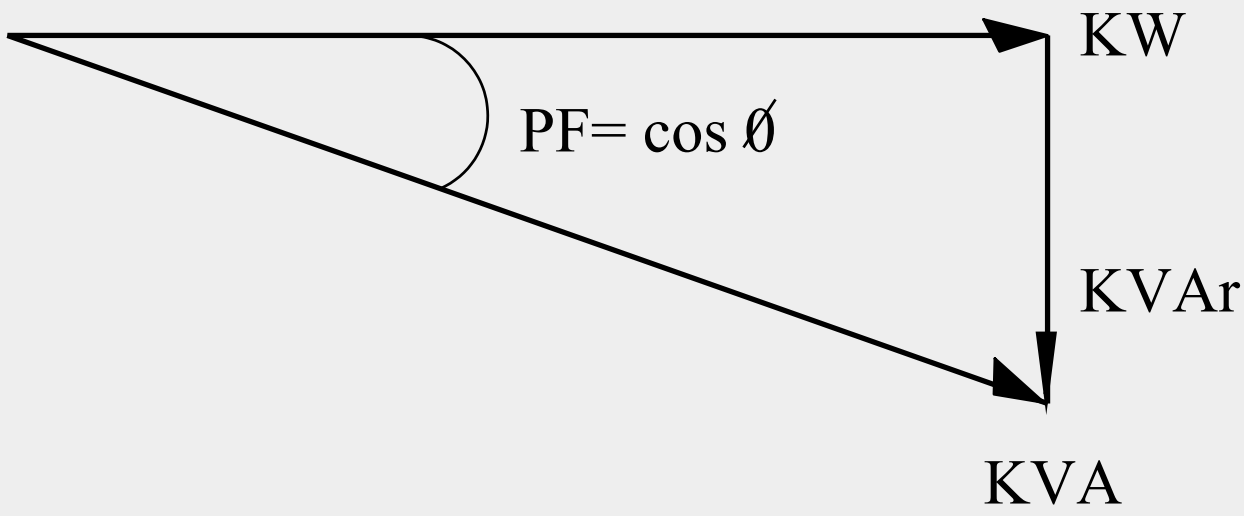
Power Factor Control In Electrical Systems.



Problems Due to poor Power Factor

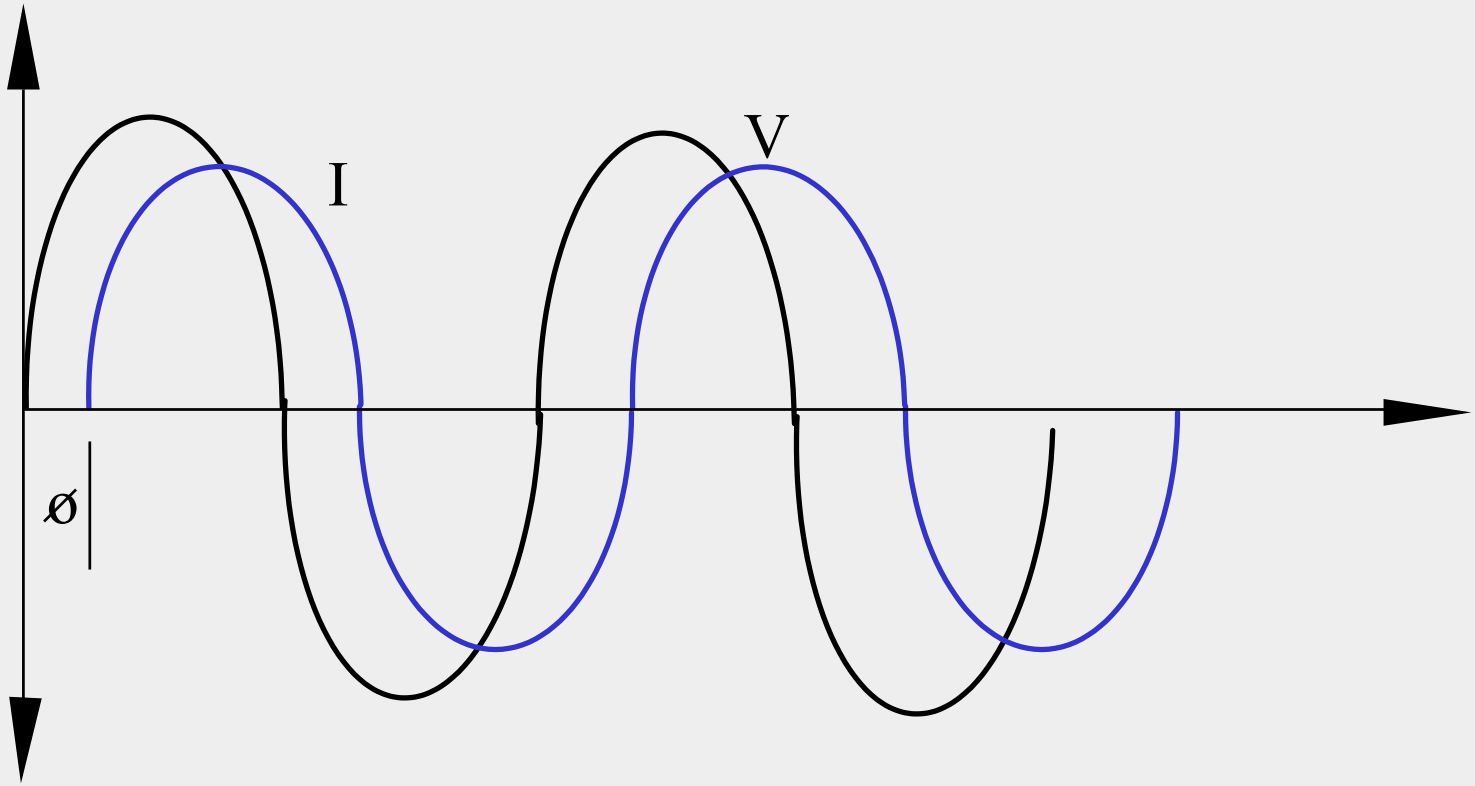
- Extra Losses in Transmission and Distribution Networks.
- Overloading the Supply System
- Increase in Maximum Demand.
- Poor Voltage regulation.
- Supply Network instability.

Phasor Diagram Showing the Effect of lagging P.F.



Power Factor is Real (Actual) Power divided by the Apparent Power. i.e. KW/KVA = P.F.

Waveforms for the Voltage and Current Showing Lagging Power Factor.

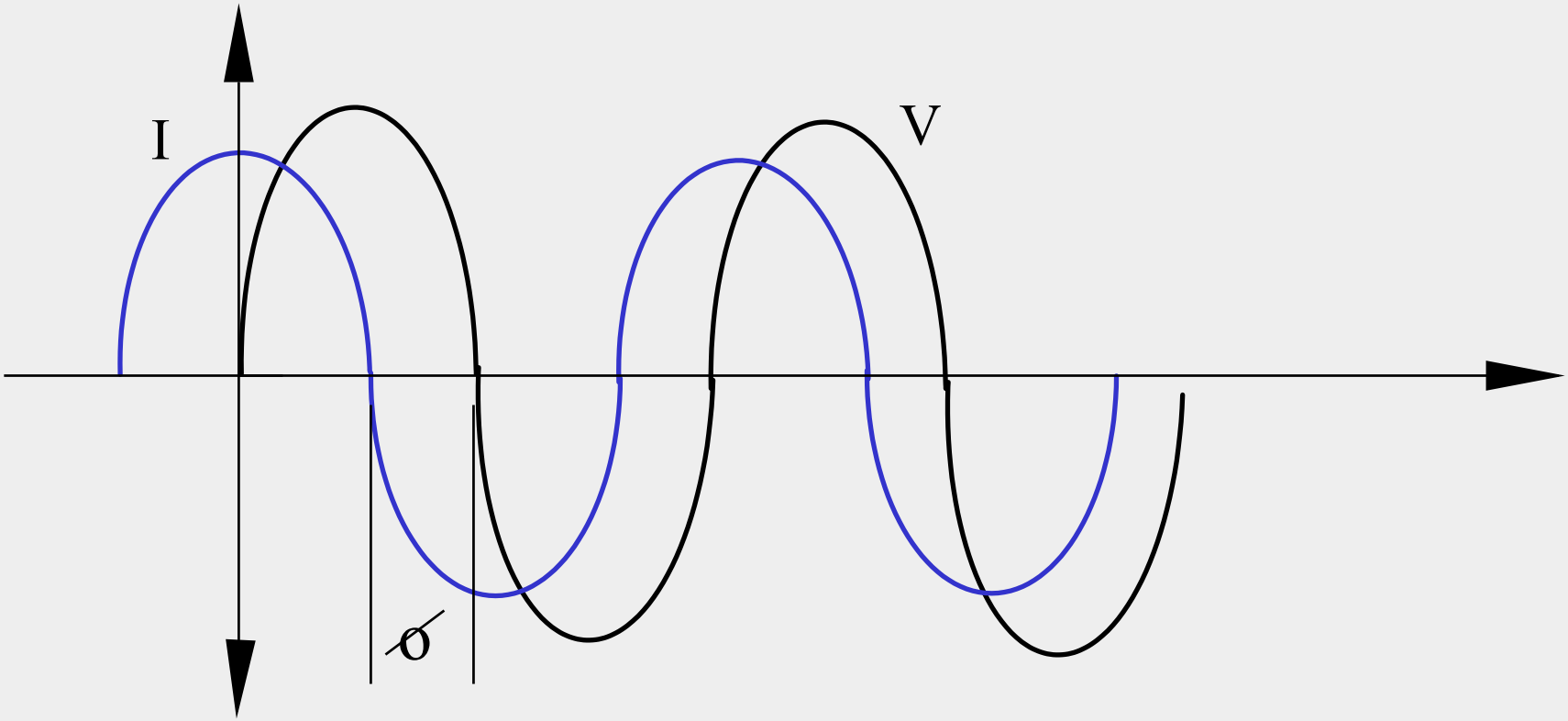


Power Factor (P.F.) = $\cos \phi$ (as the waveforms are sinusoidal)

Lagging current causes in Electrical systems.

- Highly inductive loads.
- Induction Furnaces.
- Underloaded Induction Motors.
- Fluorescent Lamps.
- Transformer NO LOAD.

Waveforms for the Voltage and Current Showing Leading Power Factor.

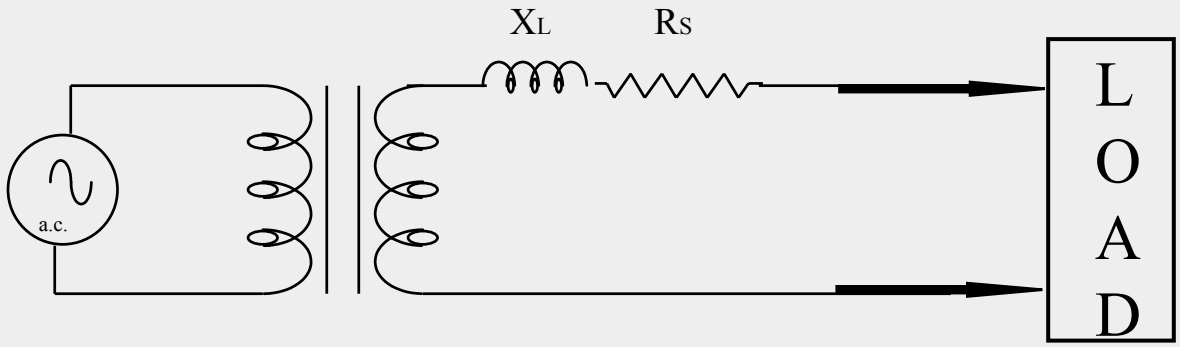


Power Factor (p.f.) = cos Ø

Reasons for Leading Current in Electrical System.

- Excess Capacitive loading in the circuit.
- Electrolysis type of loads.(Laminating)
- Underloaded Synchronous Motors.

Now lets consider the case of a typical Transformer.

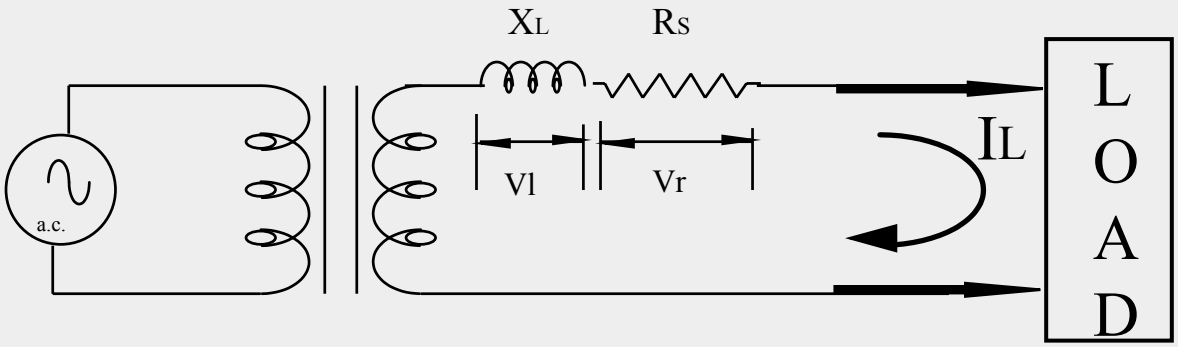


Here X_L is series inductive leakage reactance of the Transformer and R_S is the series resistance of the Transformer.
For all the practical Transformers , $X_L >> R_S$. (Normally 5 to 50 times).

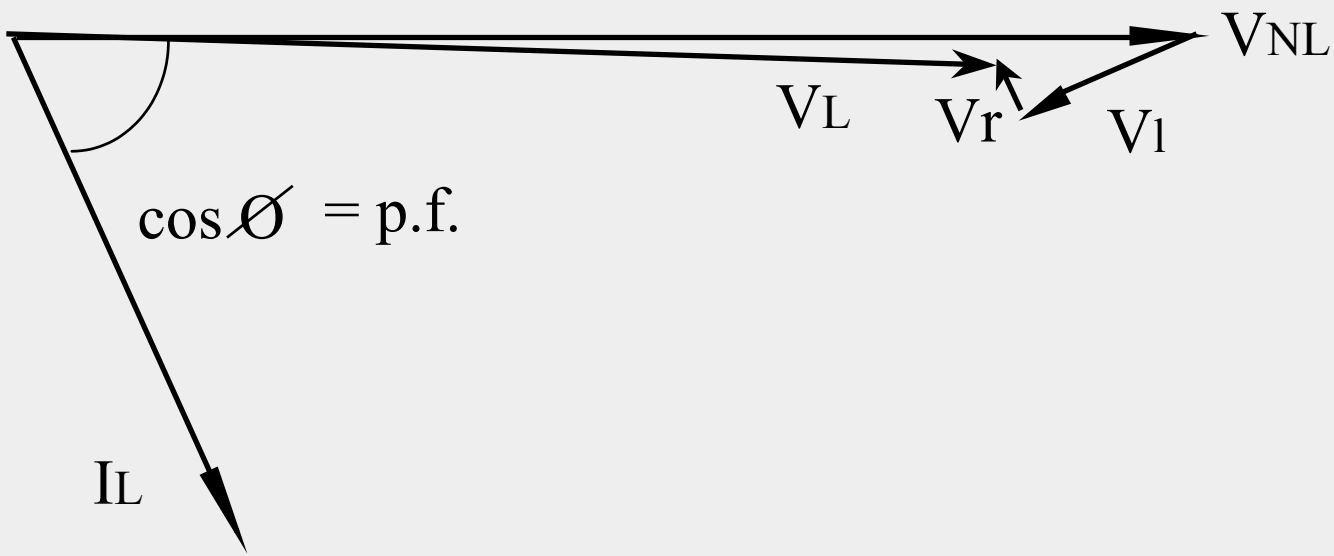
Therefore the effect of X_L on Output Voltage regulation is far more higher than the effect of Rs.

Further Shown Phasor diagrams will show the effect on output voltage in case of lagging and leading p.f. as well as unity p.f.

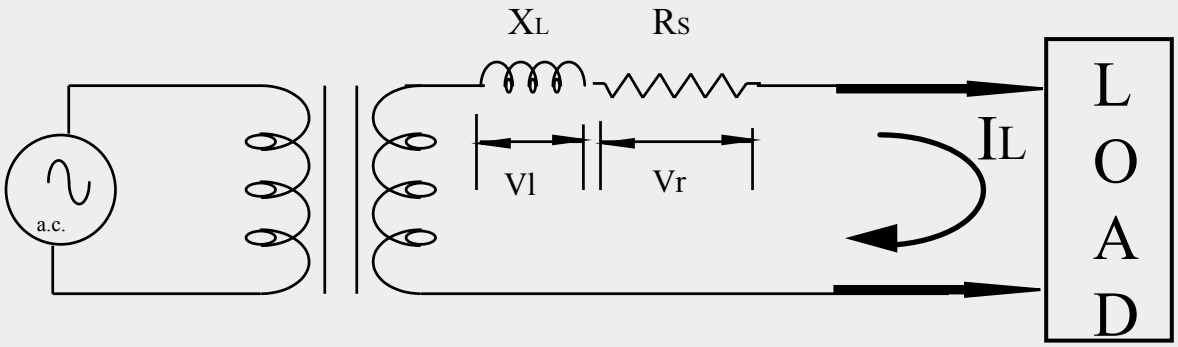
Now lets consider the case of a typical Transformer.



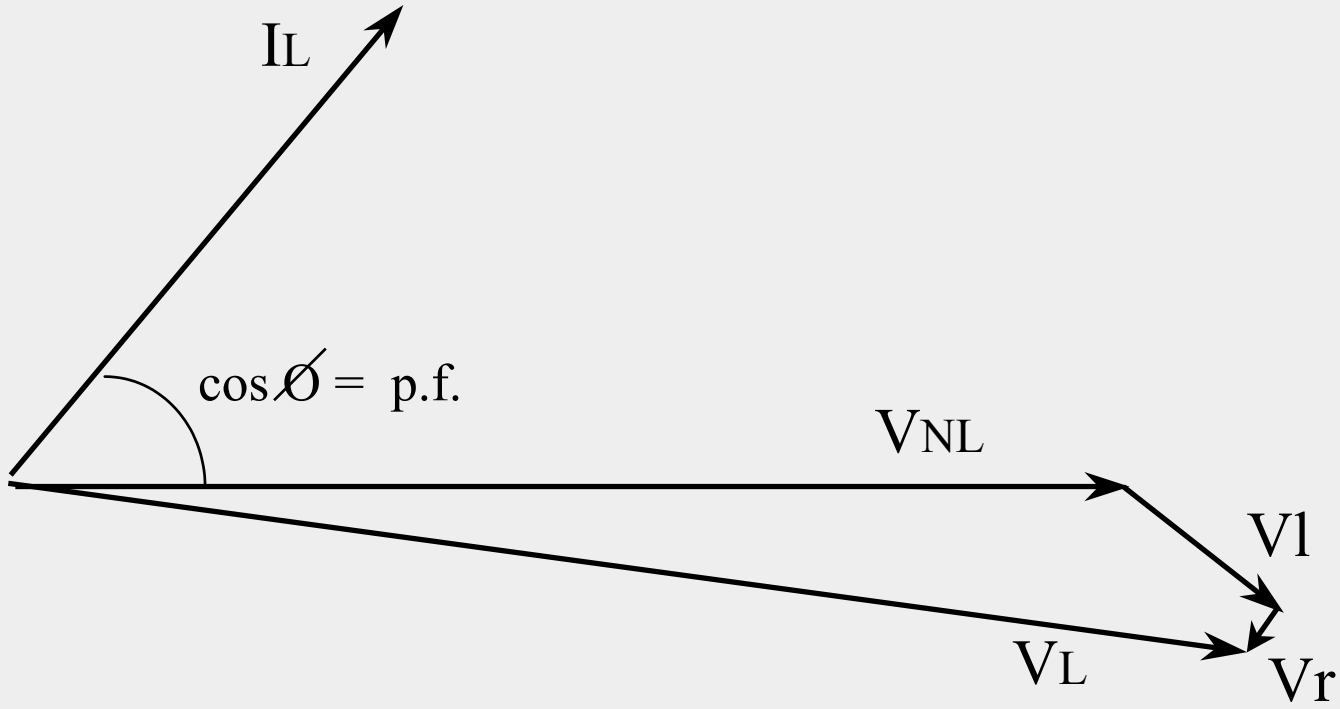
Effect of Very poor lagging power factor.



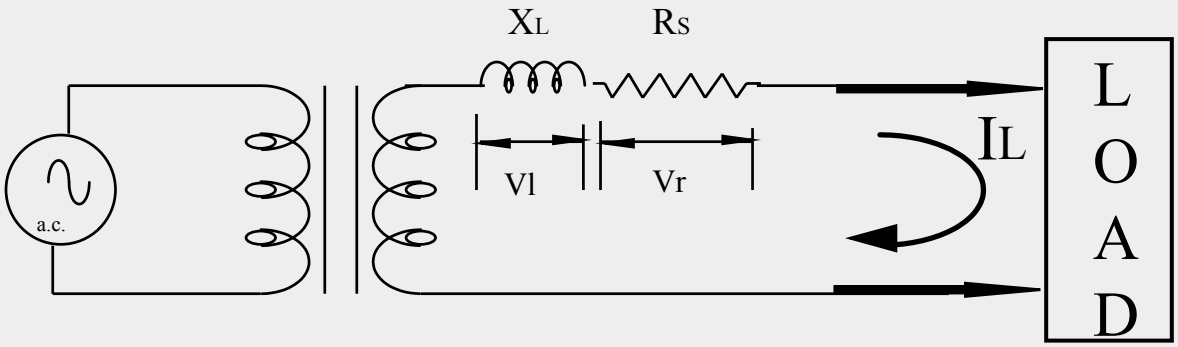
Now lets consider the case of a typical Transformer.



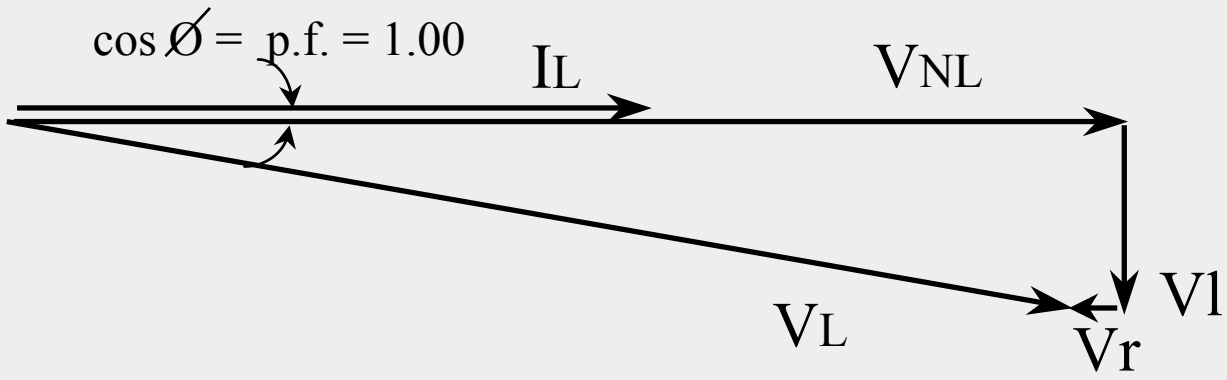
Now, lets consider the case with leading p.f.



Now lets consider the case of a typical Transformer.



Now, consider the case with almost unity p.f.



This clearly indicates the effect of poor p.f. on Voltage.

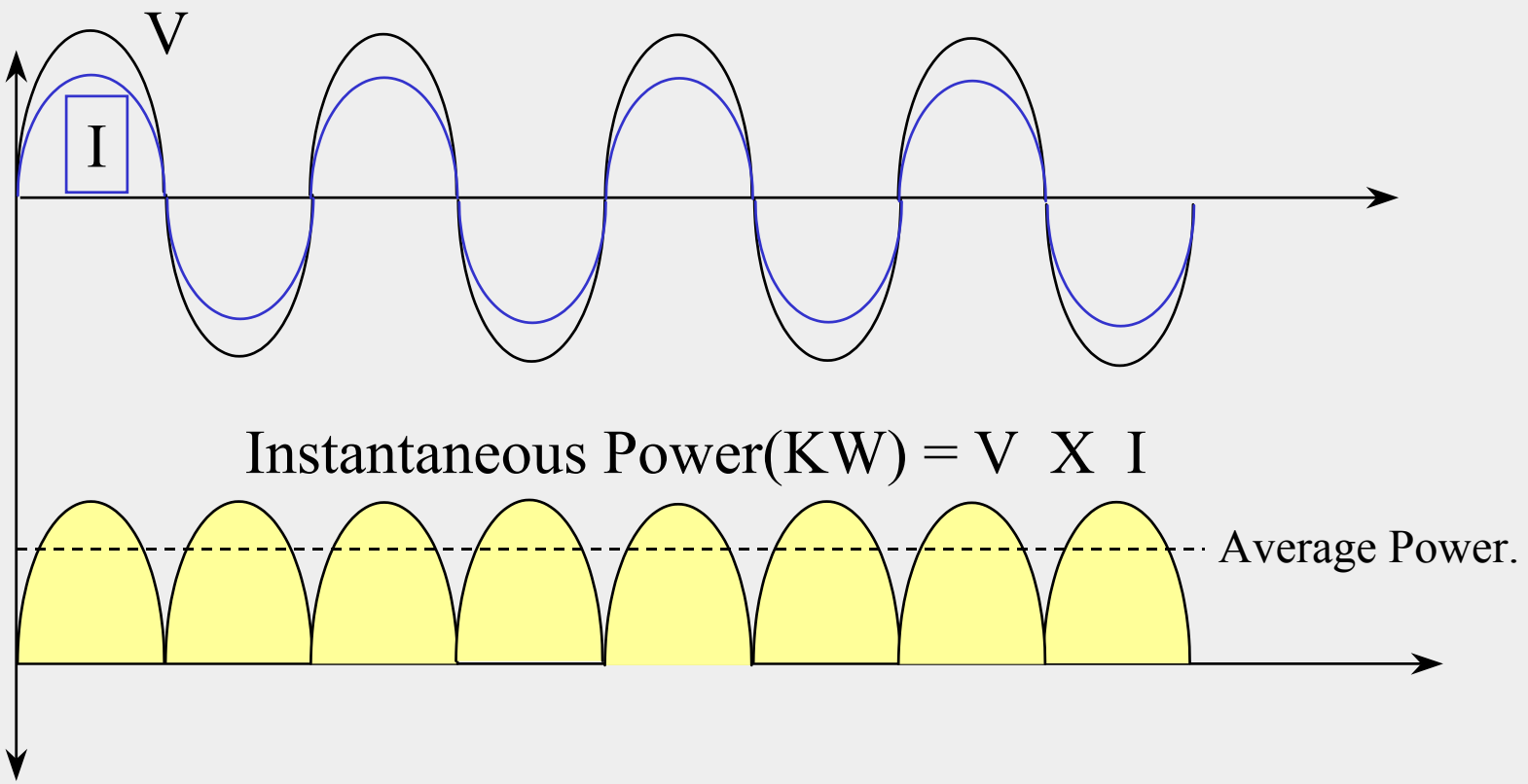
Lagging p.f.(Inductive load) causes the undervoltage problems.

Leading p.f.(Capacitive load) causes the overvoltage problem.

With p.f. near unity, voltage regulation is comparatively very good.

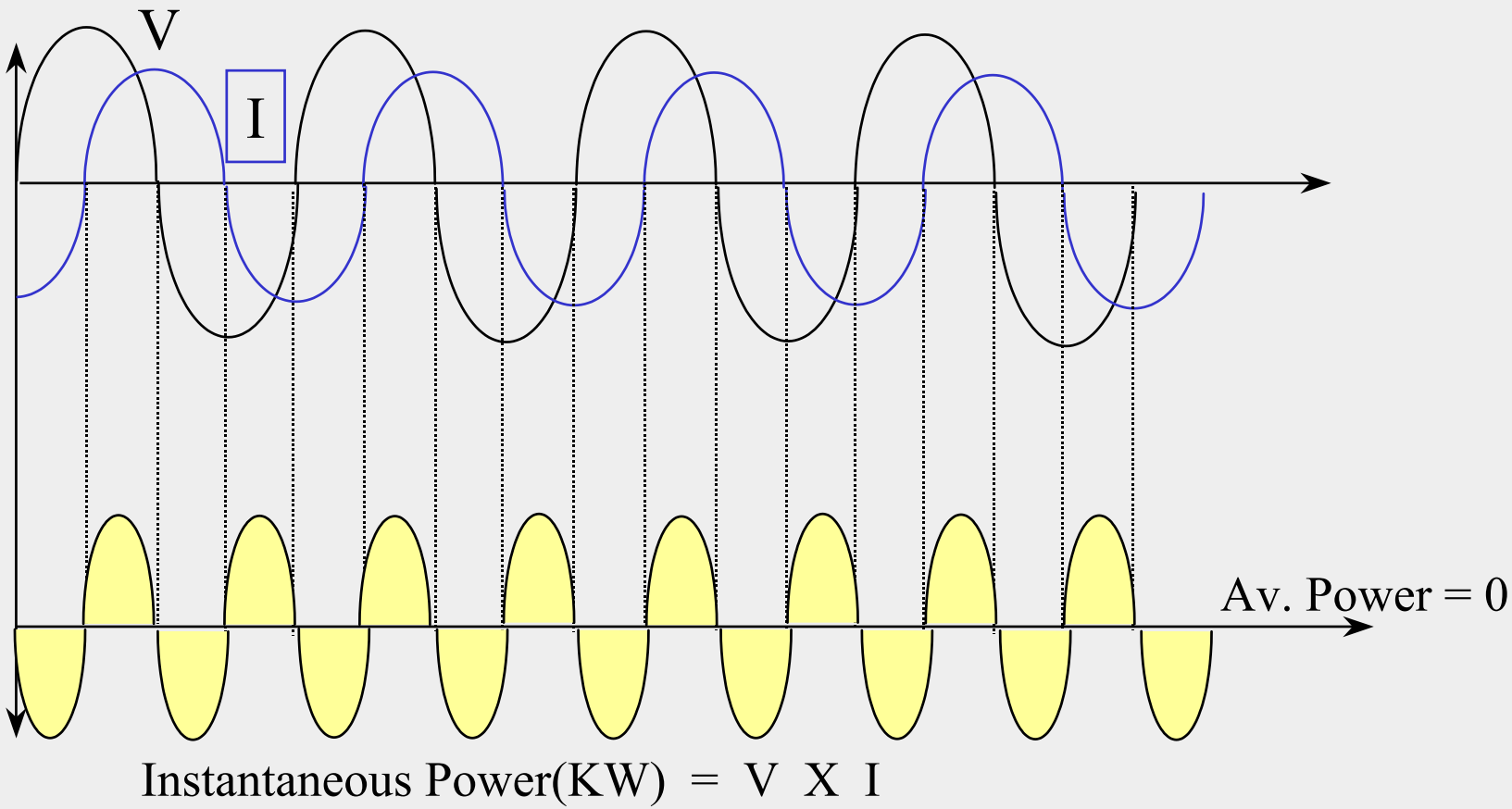
Why Power(KW) is zero with purely reactive loads.

Consider the first case with resistive load.
Here the current and voltage instantaneous value multiplication is always positive as shown in the fig. below.

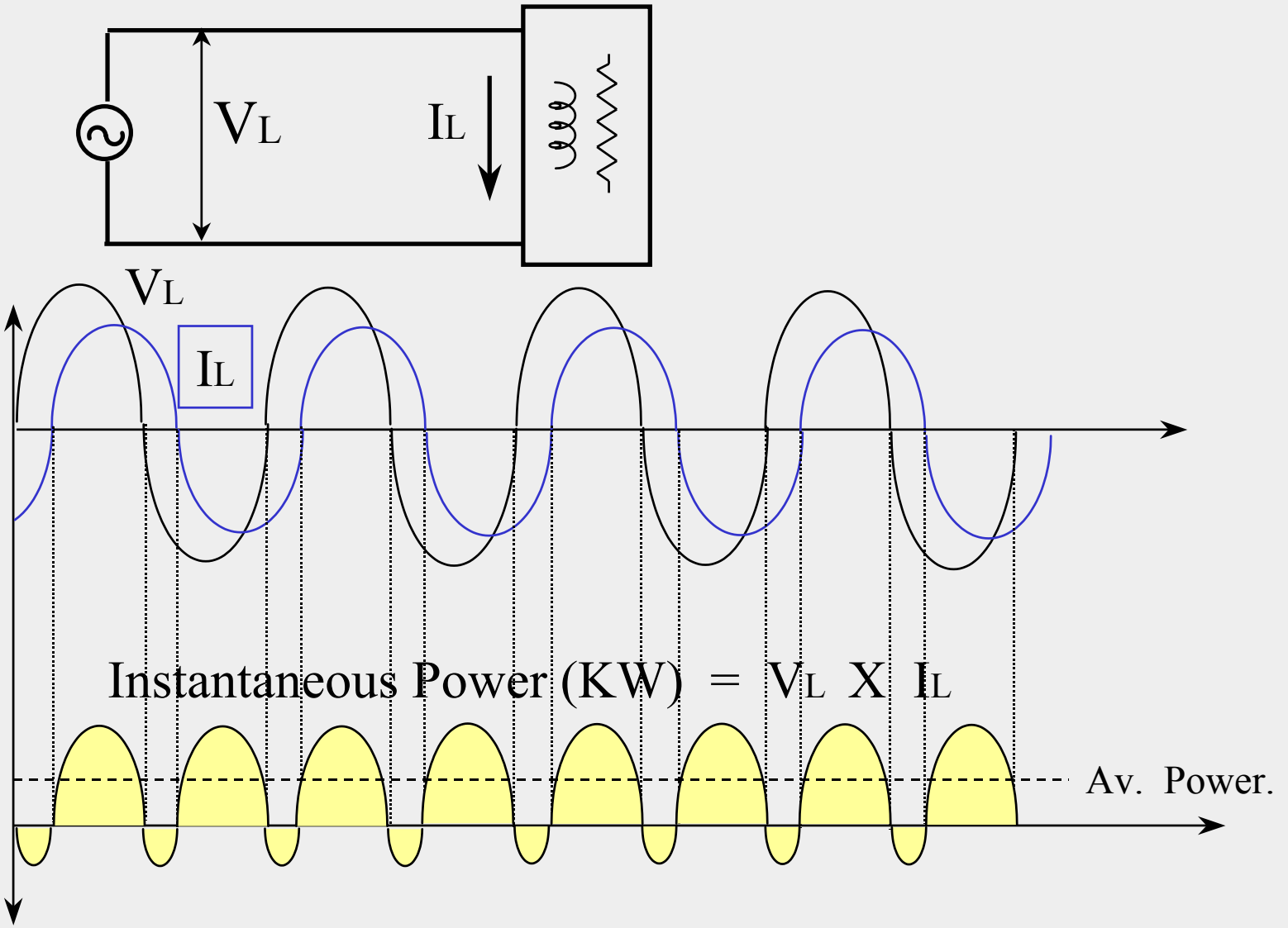


Why Power(KW) is zero with purely reactive loads.

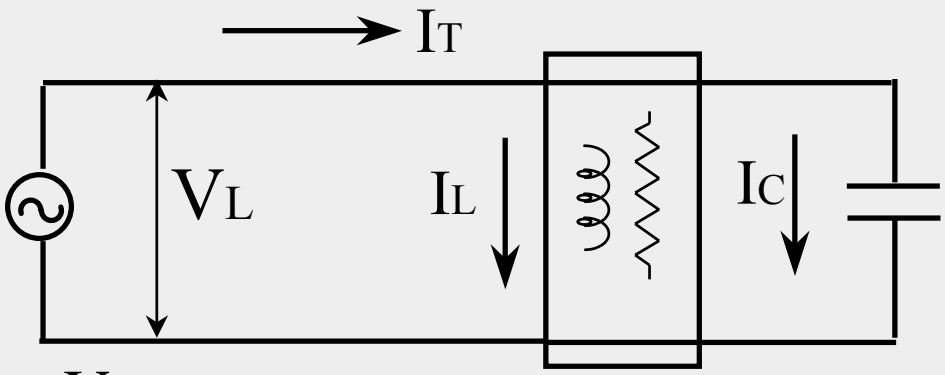
Next let us consider the case with purely inductive load. Here, the Voltage and Current waveforms has a phase angle difference of 90Deg.



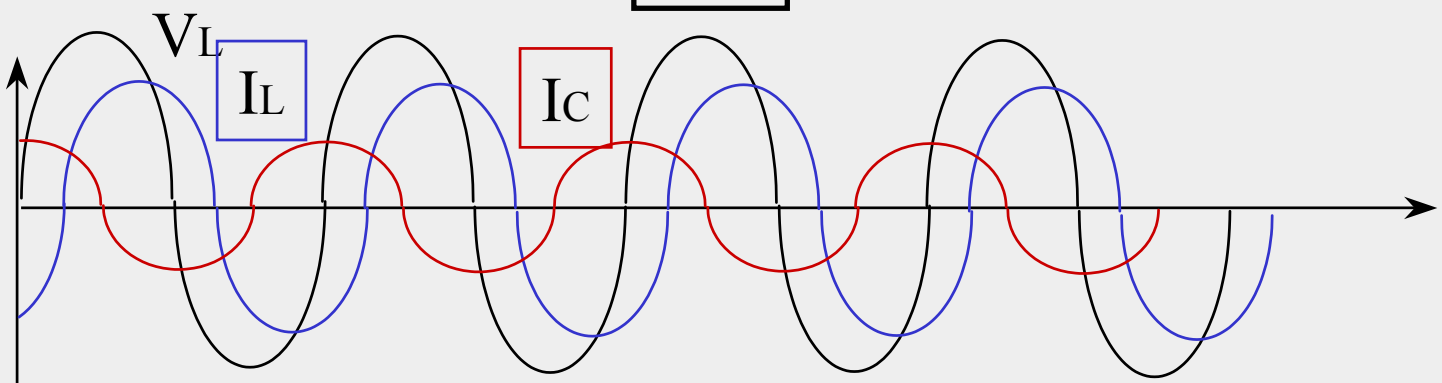
With inductive + resistive Loads

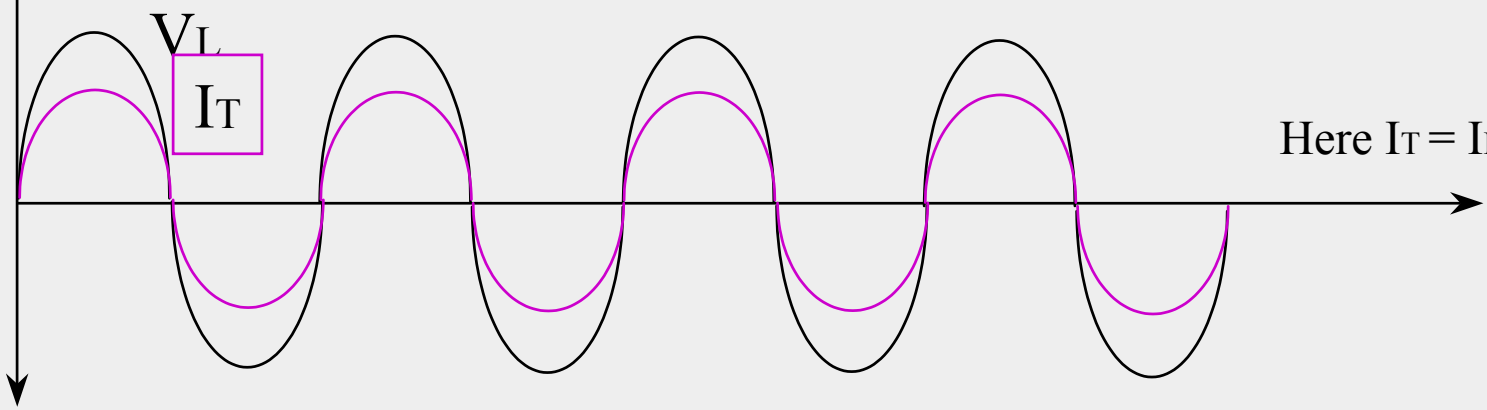


Now lets consider the effect of capacitive load .



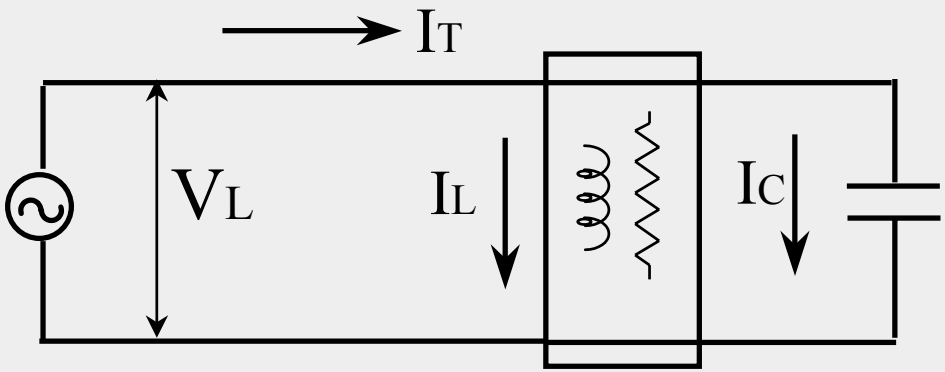
Say a capacitor is added to this circuit.





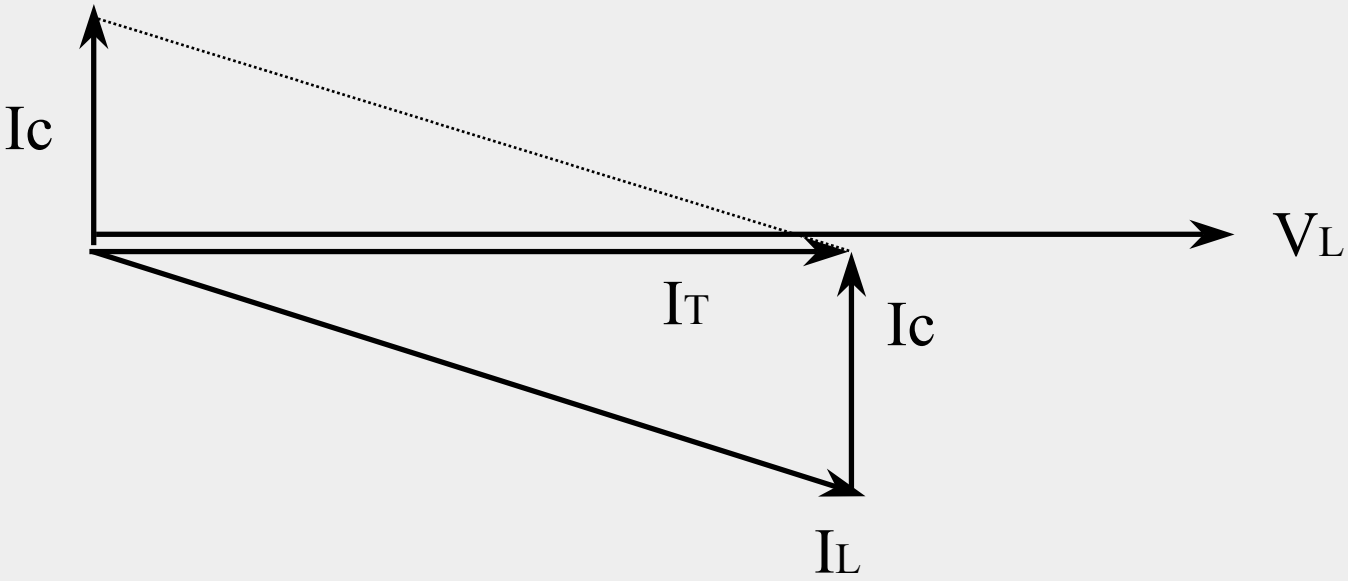
Here $I_T = I_L + I_c$

Now lets consider the effect of capacitive load .

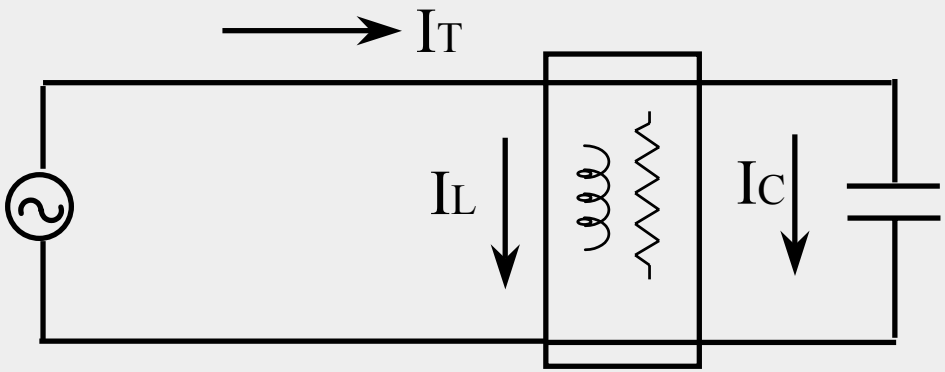


Say a capacitor is added to this circuit.

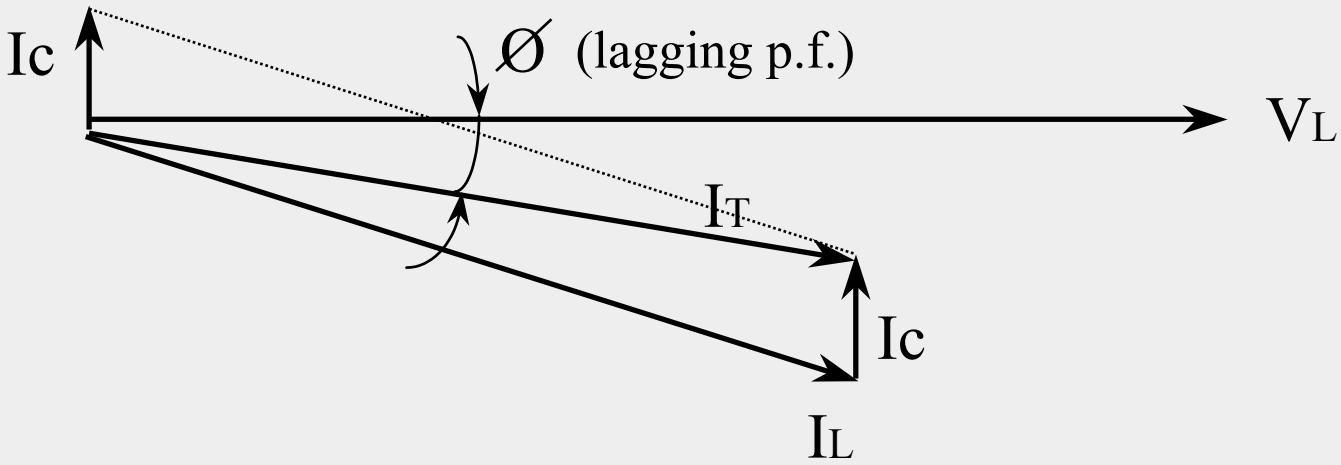
Same can be seen by the phasor diagram representation as shown below.



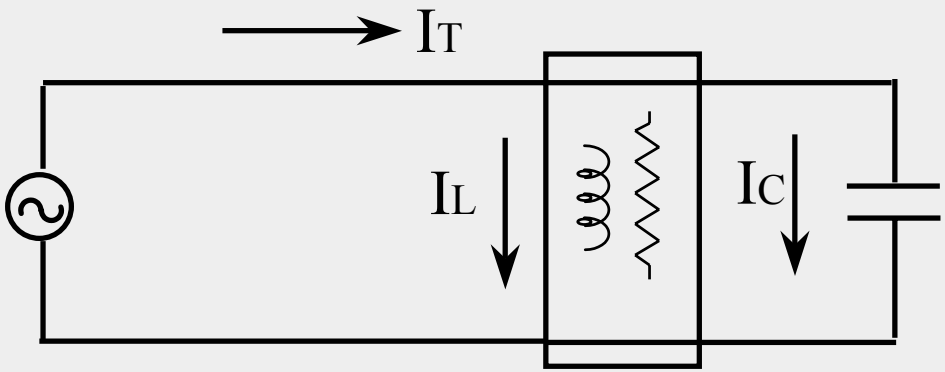
Now lets consider the effect of capacitive load .



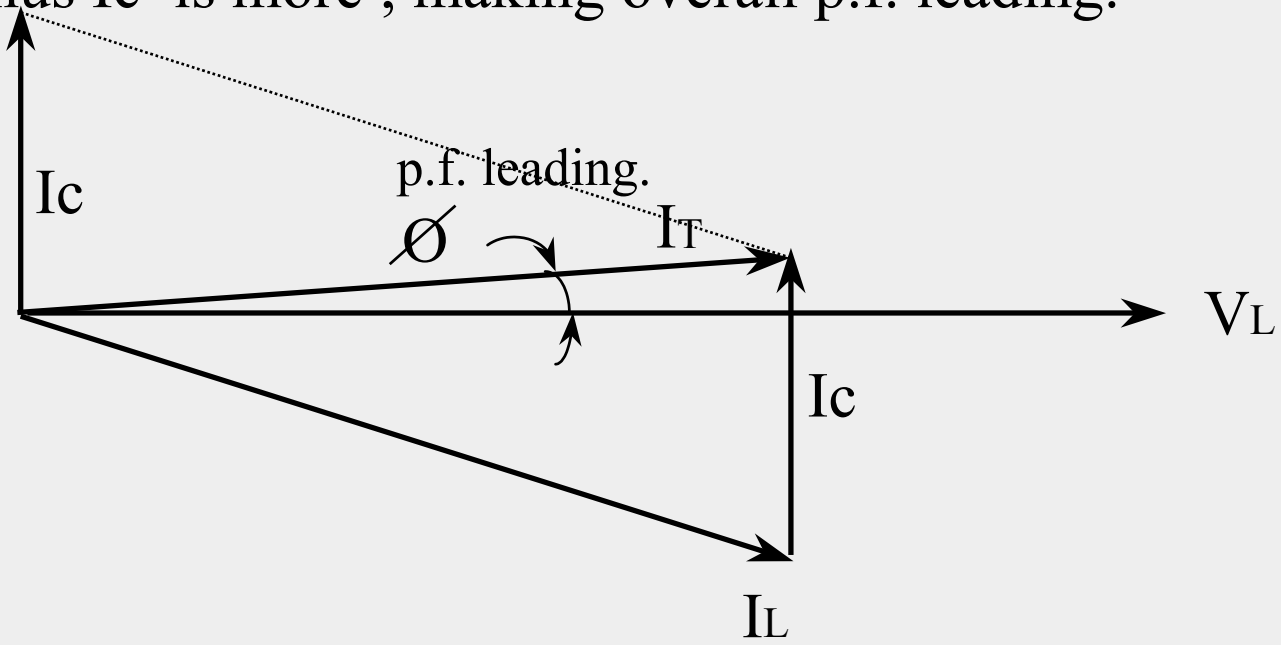
consider if the Capacitance inserted is lesser value, then Ic will be less , In that case p.f. will be lagging ≠ 1.



Now lets consider the effect of capacitive load .



Next , lets consider that more capacitance is inserted thus Ic is more ; making overall p.f. leading.



This Phasor representation clearly shows that

to maintain power factor near unity for inductive

loads;

It is very essential that the correct value of capacitor

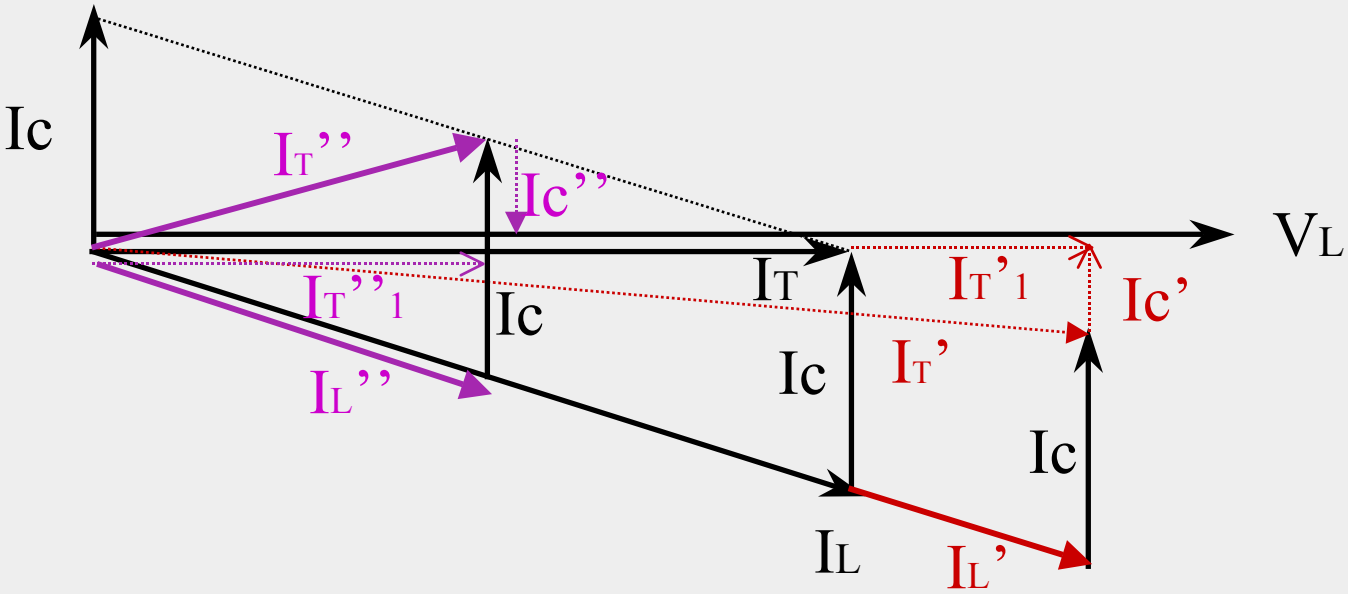
needs to be inserted in the circuit.

Consider the following phasor diagram.

Here it is seen that the capacitor compensation is perfect to give the unity p.f.

What will happen if the load changes. (initially consider it increasing.)

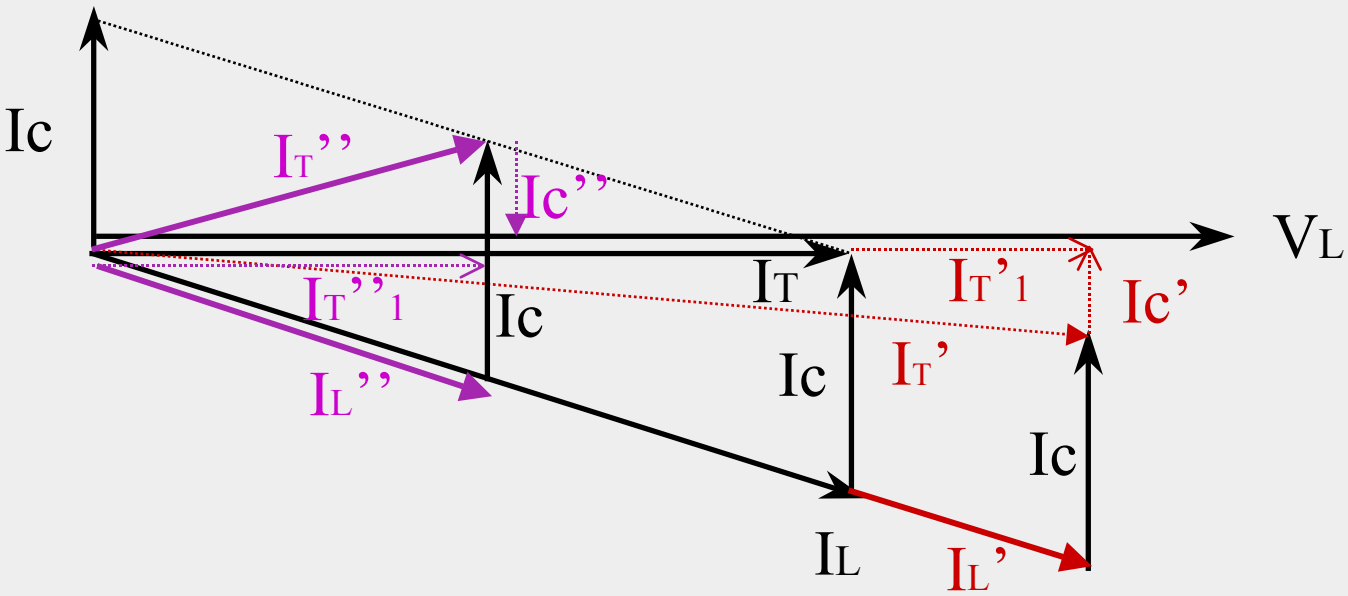
(now consider it is decreasing.)



Consider the following phasor diagram.

- This shows that even if av.p.f. is near unity, instantaneous p.f. may be different.
- Fixed compensation can give rise to extra kVA max. demand.
- During less loading, due to leading p.f. overvoltage can occur.
- Fast changing loads can give rise to sudden voltage fluctuations.

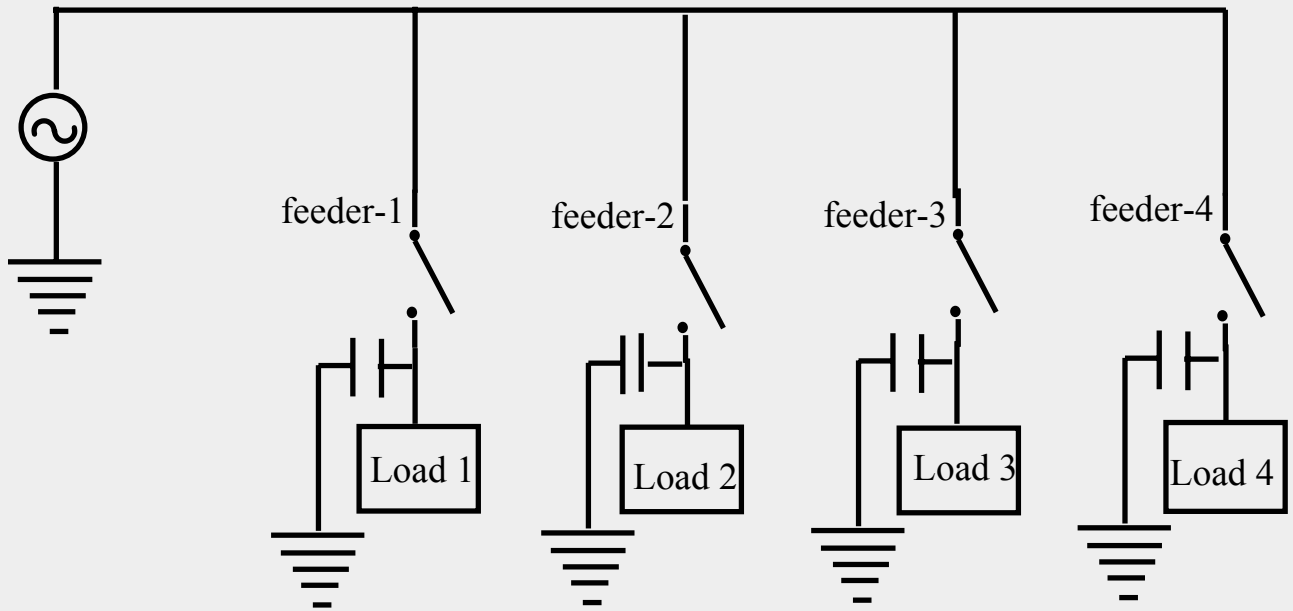
- **Thus fast correction of p.f. is very much necessary.**



Methods of Improvement of P.F

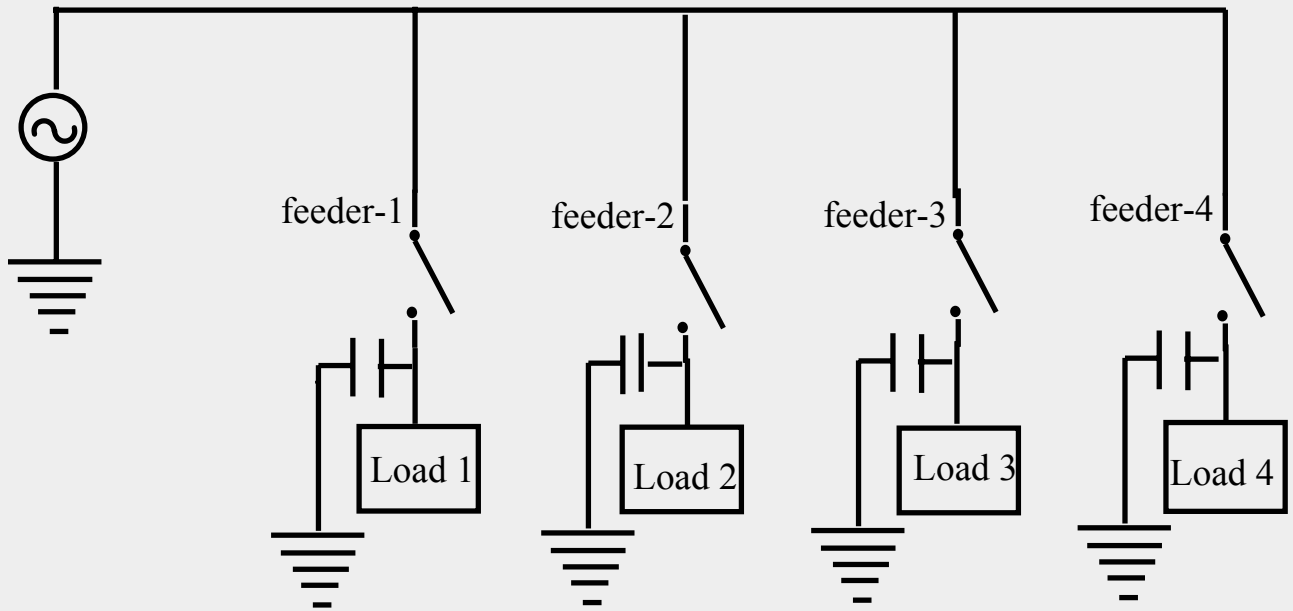
- Use of correct capacity induction motors, instead of using overrated motors
- Possible use of synchronous machines wherever possible
- Usage of capacitors of proper capacity to compensate inductive current, by capacitive current

The best way to control the p.f. is to connect the capacitors of correct KVAr value nearest to the individual loads.



Here , every load is connected with just correct value of capacitor across it. So, when the load is put on, the capacitor also comes into the circuit.

The best way to control the p.f. is to connect the capacitors of correct KVAr value nearest to the individual loads.



But still, this way of compensation becomes unpractical in terms of maintenance, safety and space.
Therefore this method is normally not adopted.

Use of Synchronous machines for P.F. improvement Has following draw-backs. Thus is not very much a preferred method.

- Very high cost of the equipment.
- Requirement of extra prime-mover to start the machine.
- If the machine is used only for p.f. improvement then in such case, machine losses are comparatively very high.
- Very high cost of maintenance.
- Possibility of more breakdowns due to moving parts.

The most popular method for P.F. improvement is the use of capacitor switching panel.

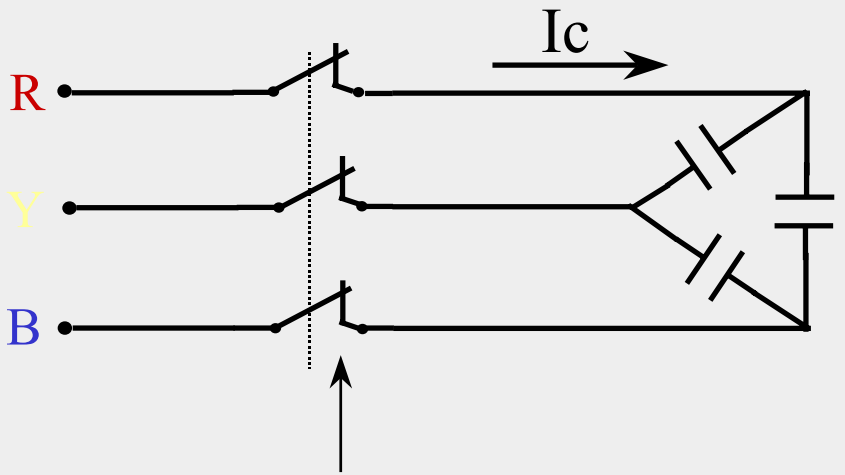
- Easy to maintain.
- Gives desirable results.
- Cost effective.
- More safe for usage.
- Very less down time.

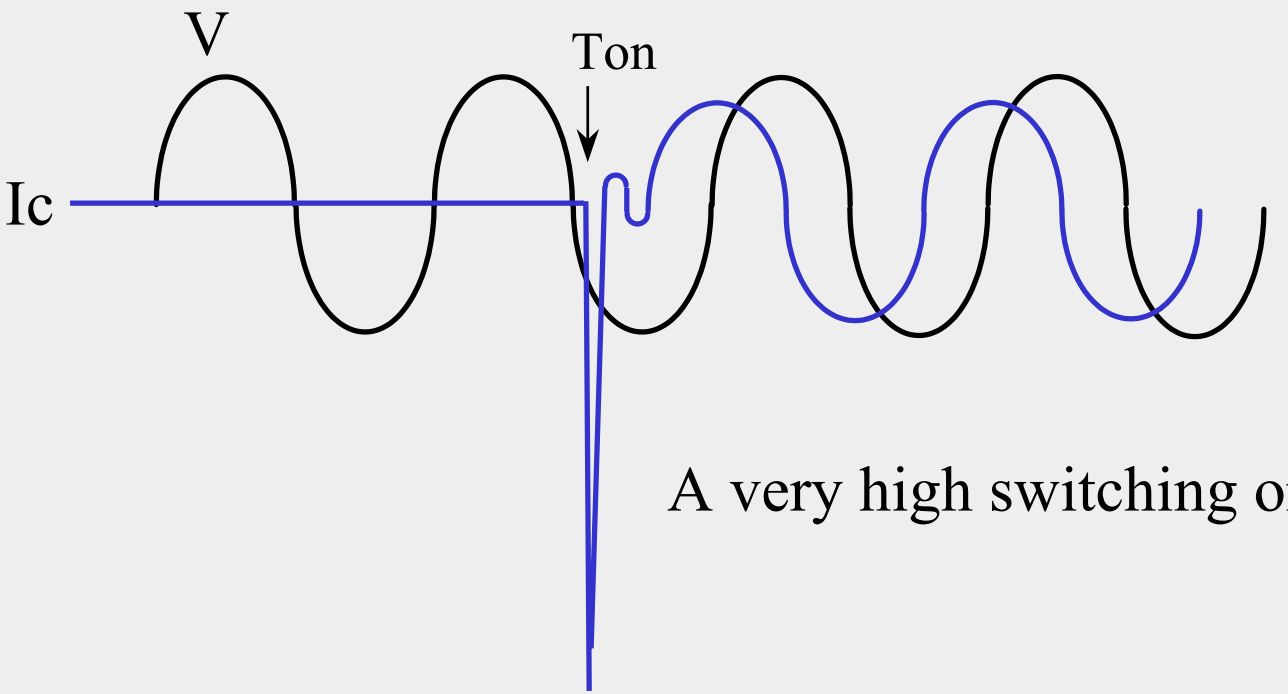
The Capacitor Switching Panel uses various methods for switching on the capacitor banks.

These methods can be broadly catagorised as:-

- Direct on line contactor switching.
- Double contact contactor switching.
- Thyristorised switching.
- Capacitance control using PWM technique.

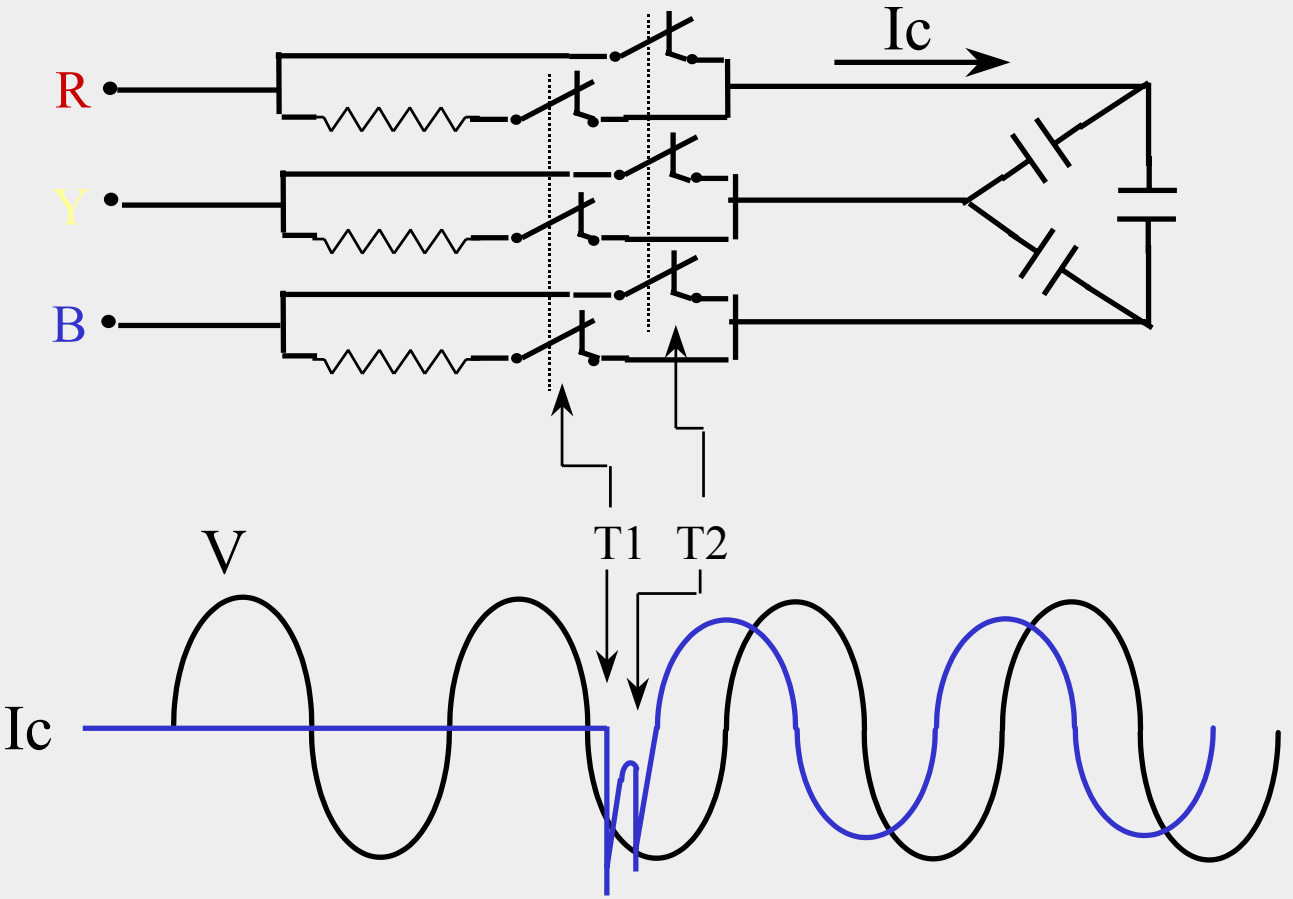
Direct on-line Contactor Switching.





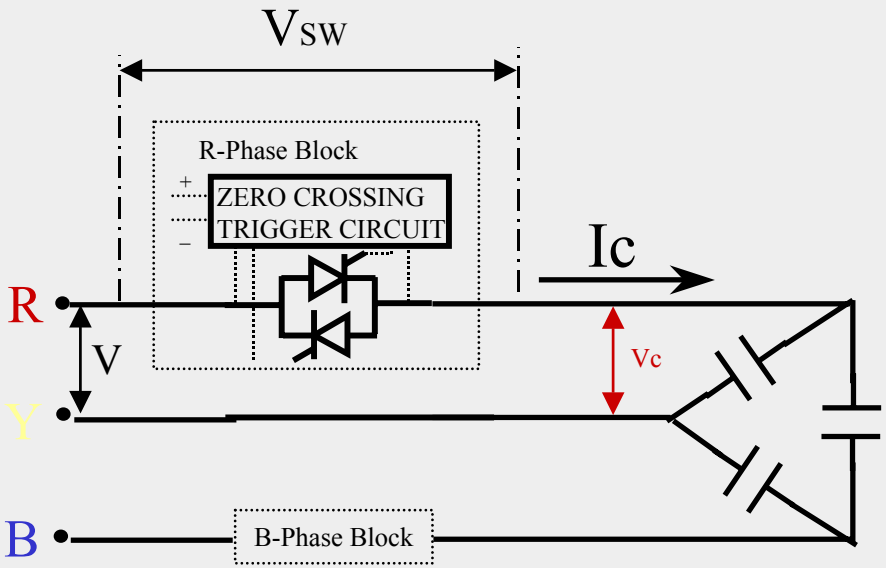
A very high switching on surge current.

Double contact Contactor Switching

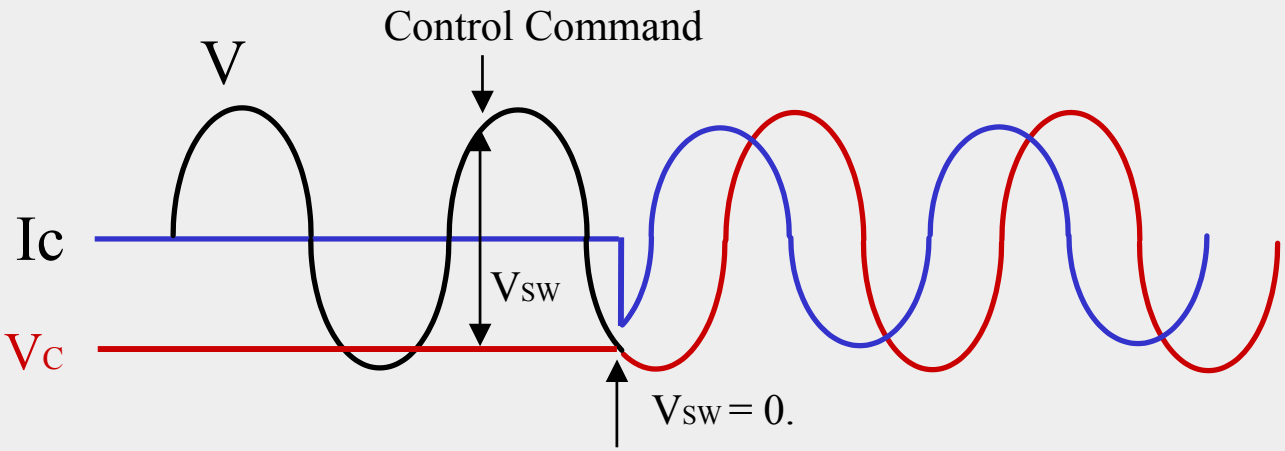


Switching surge current is reduced and controlled but not totally eliminated.

Thyristorised Switching (with zero crossing detect)



This clearly shows that the thyristorised switching along with the zero crossing detect circuit will bring the switching surge currents to almost nil.



Capacitance Control using PWM technique.

- By far the best method known for capacitance control.

But still today, not much commercialized.

Design involves high speed switching, high powered semiconductor devices like I.G.B.T.s.

Single capacitance bank is used for the entire control purpose.

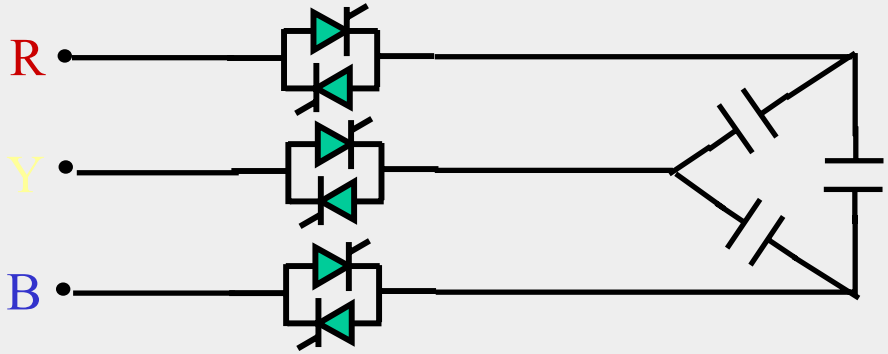
Major drawback is Very high cost of the equipment.

Thus so far known proven best method is Thyristorised switching.

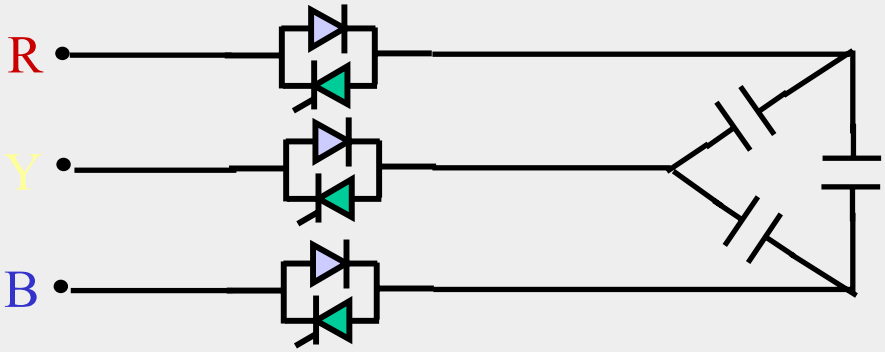
There are various configurations in which the thyristor blocks can be connected in the power circuit.

These are as follows.

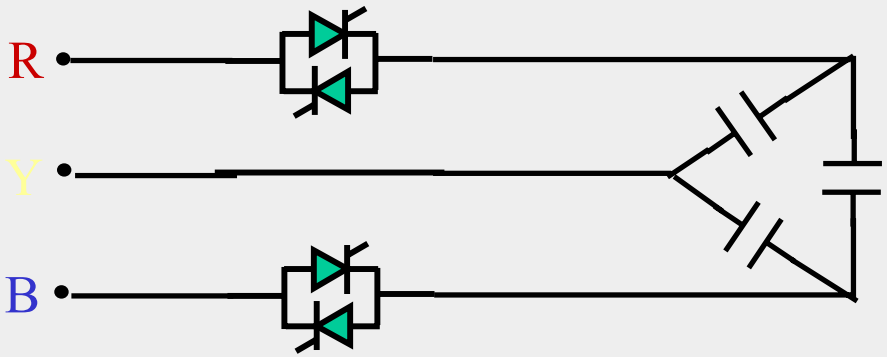
- **Back to back thyristor blocks in all the three phases.**
- **Back to back thyristor and diode block in all the three phases.**
- **Back to back thyristor blocks in only two of the three phases.**



Back to back connected Thyristor blocks in all 3 Phases.



Back to back connected Thyristor and Diode blocks in all 3 Phases.



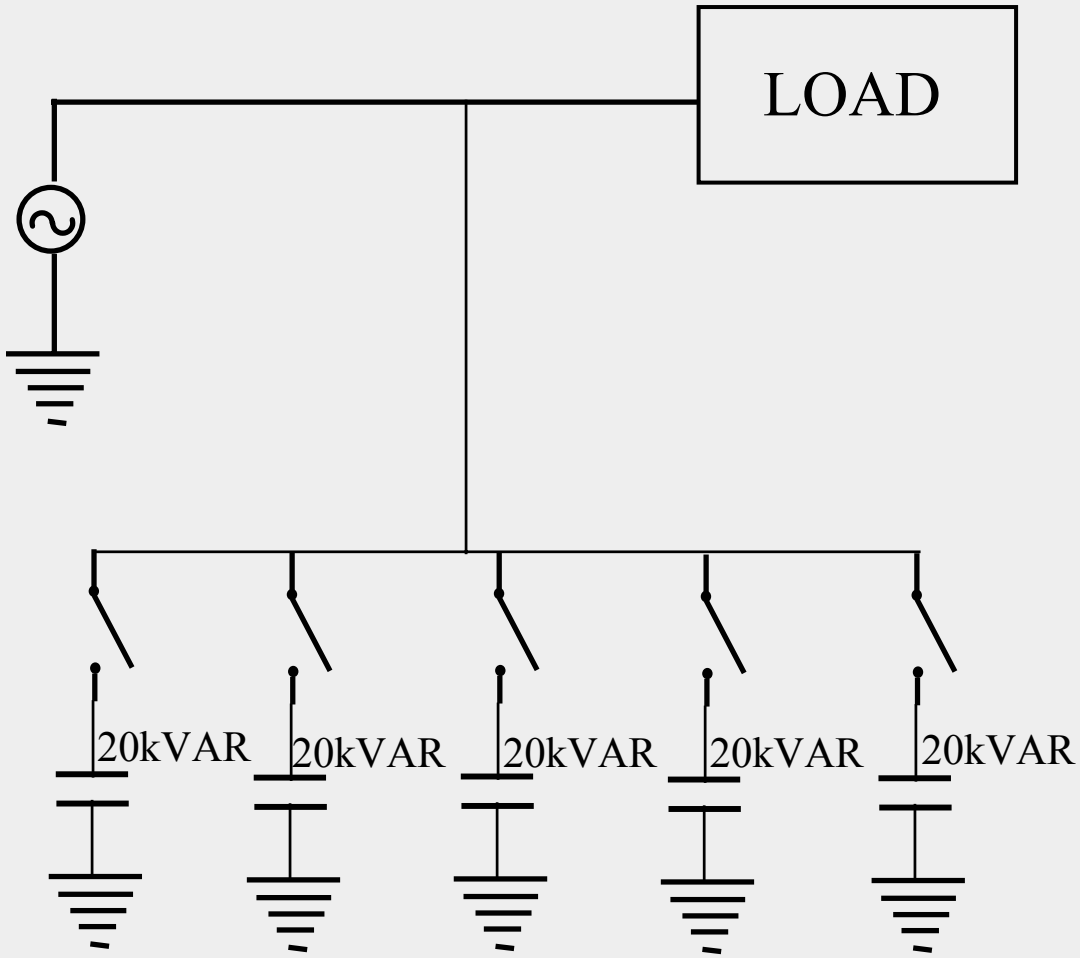
Back to back connected Thyristor blocks in only 2 out of the 3 Phases.

SWITCHING CONFIGURATIONS ARE OF TWO TYPES.

- **Equal value switching.**

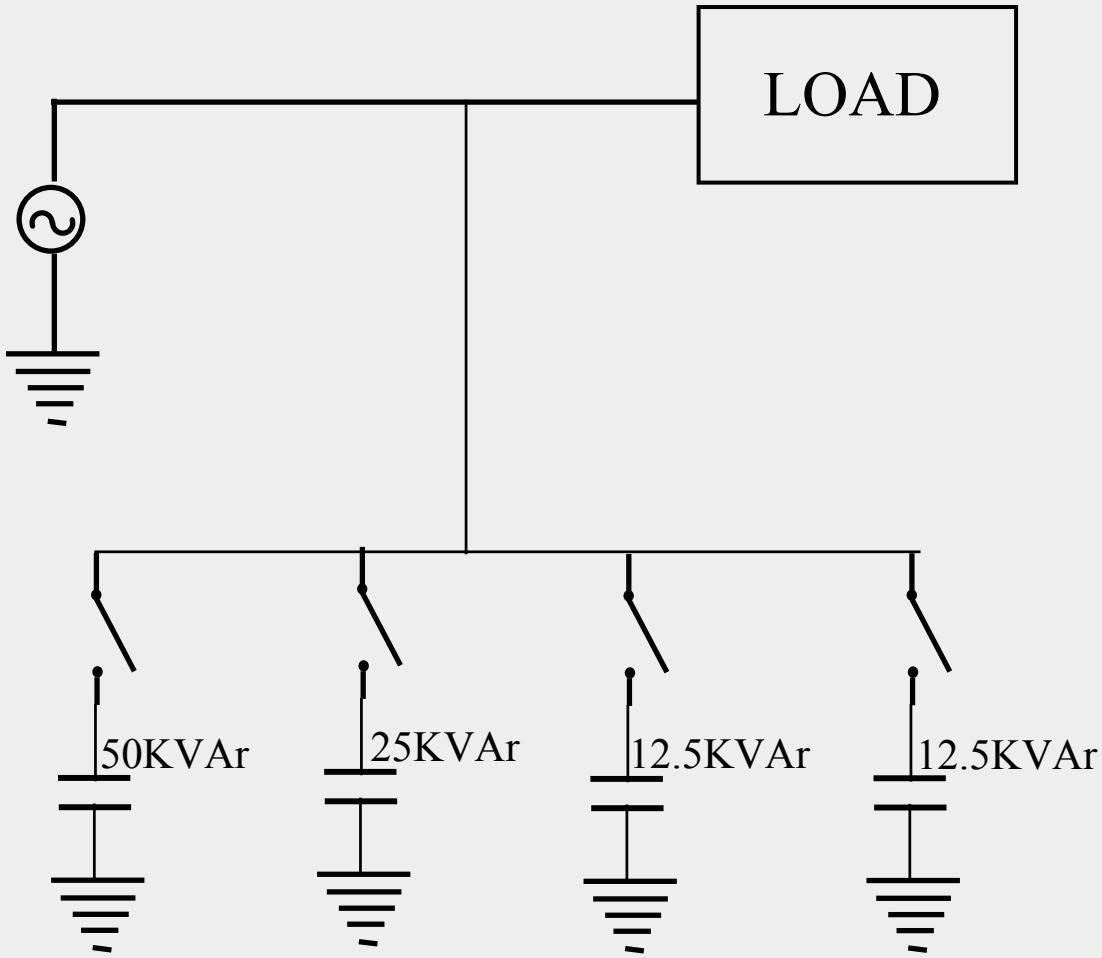
- **Binary switching.**
  - **A) Using equal smallest bank.**
  - **B) Using 2/3 and 1/3 ratio smallest bank.**

100 KVAr equal switching configuration.



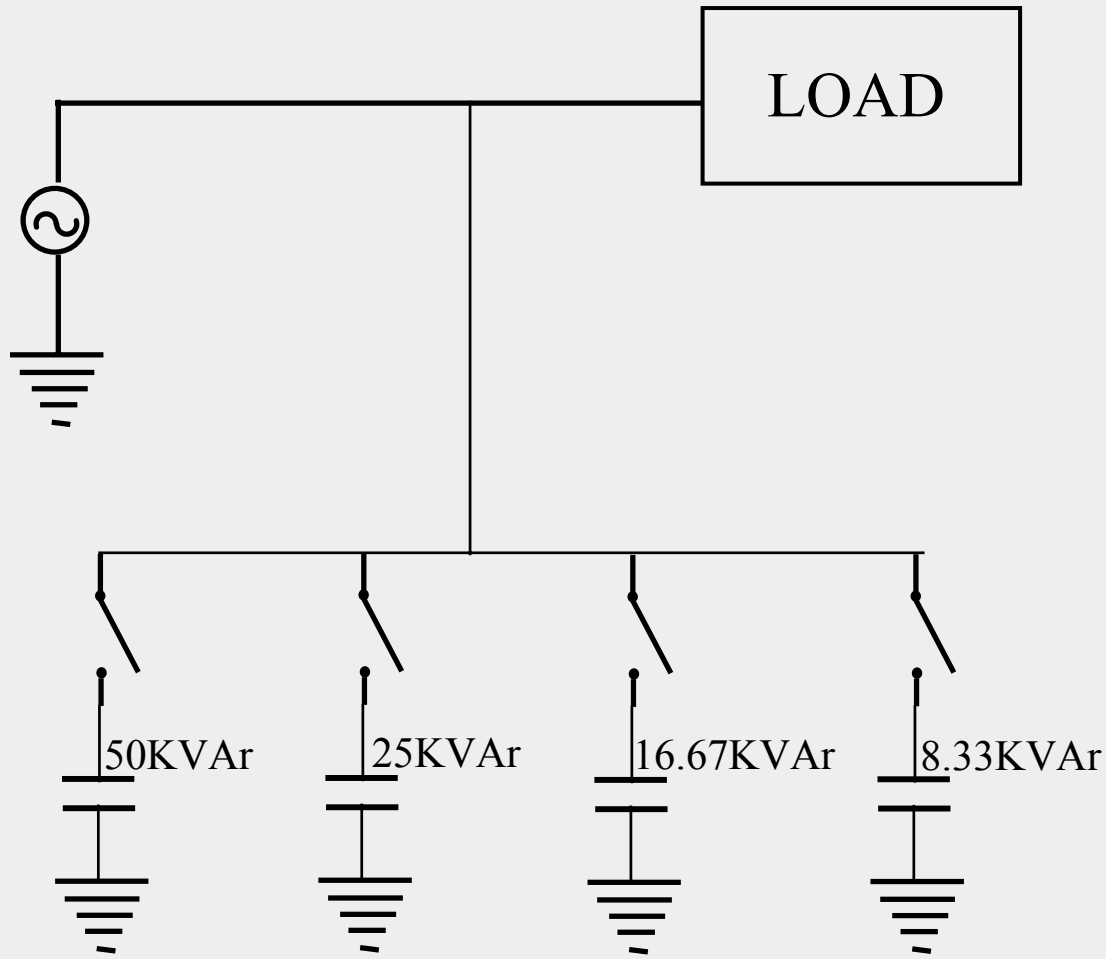
No. of switches = 5 , Resolution = 20 KVAr.

Binary configuration with equal smallest bank. For 100KVAr system.



No. of switches = 4 , Resolution = 12.5KVAr.

Binary configuration with 2/3 & 1/3 smallest bank. For 100KVAr system.



No. of switches = 4 , Resolution = 8.33KVAr.

Now Let's Consider the effect of harmonics on Capacitors.

$$\text{Capacitive impedance} = 1 / (2 \cdot \text{Pi} \cdot F \cdot C)$$

Here Pi = 3.14152., F = frequency, C = Capacitance in Farad.

Harmonics are the higher frequency components present on the supply system.

Therefore the impedance offered by the capacitors is far less for the higher harmonic components on the supply system.

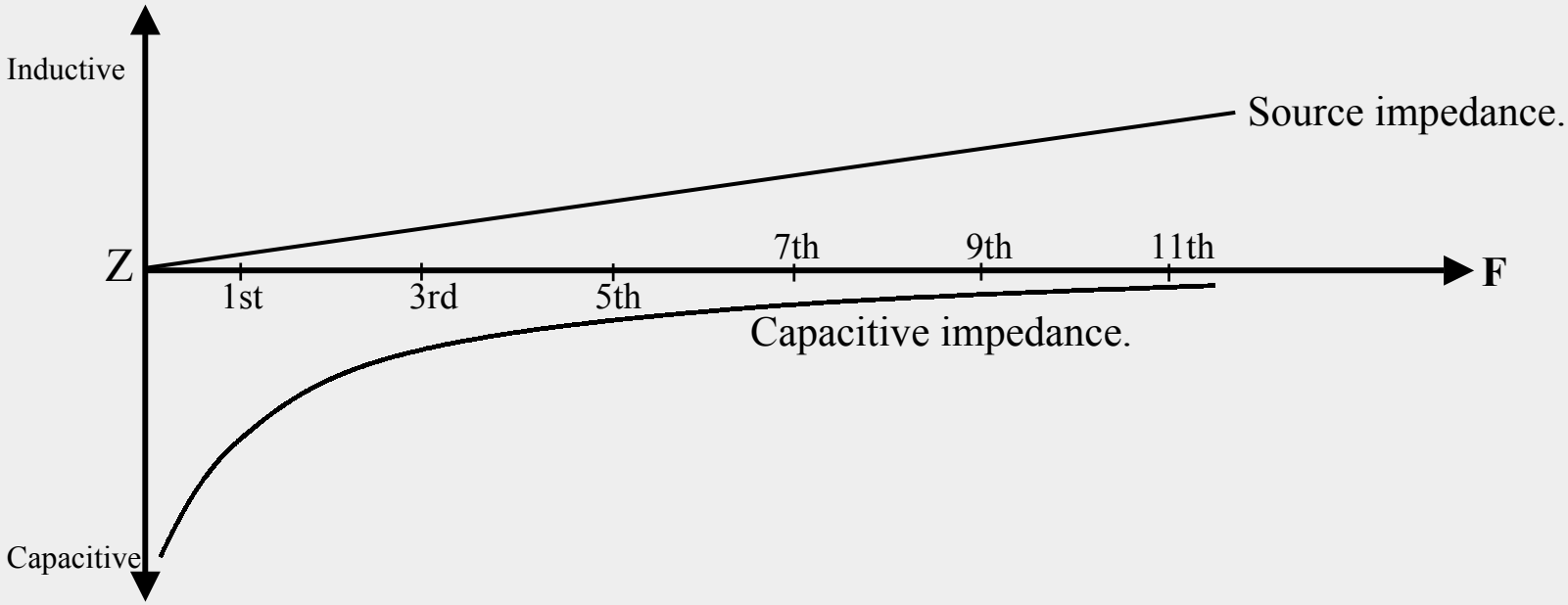
Other impedances like cable and source etc. are inductive which increases with with the frequency and starts offering more impedance with higher harmonics.

Now Let's Consider the effect of harmonics on Capacitors.

Capacitive impedance = 1 / (2 . Pi . F . C)

Here Pi = 3.14152., F = frequency, C = Capacitance in Farad.

Following impedance plot will clarify this more effectively.



As the impedances offered at higher harmonics by the capacitor are far lesser than the other circuit impedances;

Major part of the harmonic currents if present, flows through the Capacitor banks connected on the supply lines.

This causes the major problems to the capacitors.

Viz.

- Extra Dielectric losses in the capacitors.
- Overcurrents through the capacitors.
- Heating of the capacitors.
- Reduction in working life of the capacitors.
- Reduction in capacitance values in terms of Farad.
- Capacitor container blowing off causing human safety problems.

Therefore its very clear that if the load harmonics are substantial on the supply systems, the pf improvement capacitors can get damaged and there is a need to protect them.

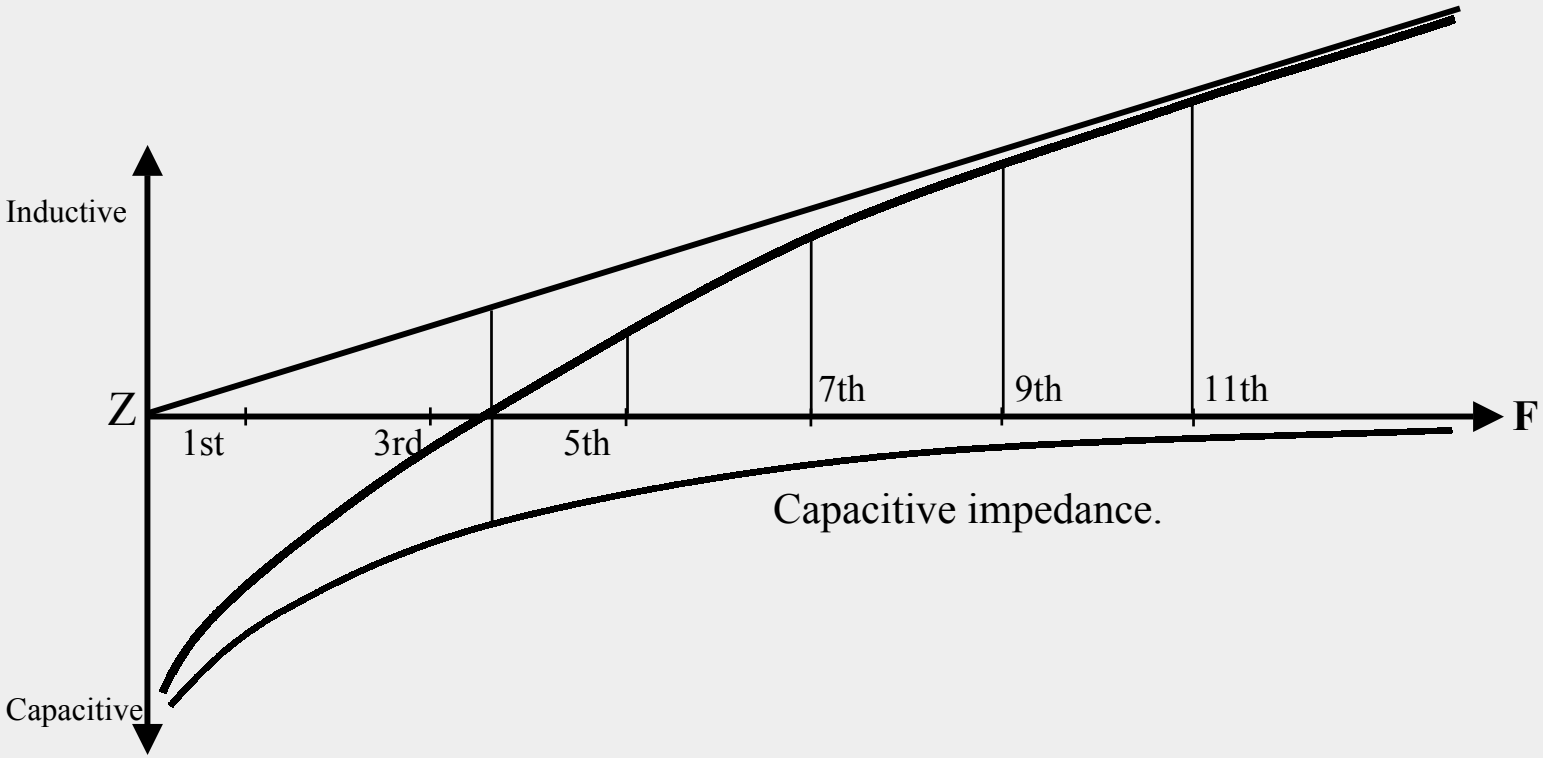
The simple method used here is that of de-tuning of the capacitors.

An inductor of suitable value is added in series with the capacitors & this make a series L-C circuit. The resonance frequency of this L-C combination is kept such that it does not match with any of the harmonic frequency or its multiples.

The typical value of this resonance frequency for 50Hz. Mains circuit is kept as 187Hz.

The impedance characteristic graph will elaborate this.

Impedance Plot for Detuned Capacitors.



It can be therefore seen that impedance value offered by detuned capacitors is far higher than what is offered by plain capacitor.

This will avoid harmonics currents to flow through the capacitor banks and provide them the protection.

TAS PowerTek

THANK YOU.